Customer No.: 31561
Application No: 10/710,671
Docket No.:13085-US-PA

REMARKS

Present Status of Patent Application

This is a full and timely response to the outstanding final Office Action mailed on January 6, 2006. The Examiner rejected claims 1-6 under 35 U.S.C. 102(e) as being anticipated by Hsieh (USP 6,645,813) and claims 7-10, 19-22 under 35 U.S.C. 103(a) as being unpatentable over Hsieh *See id.* at Pages 3-9.

After carefully considering the remarks set forth in this Office Action and the cited references, Applicants respectfully submitted that the presently pending claims are already in condition for allowance. Reconsideration and withdrawal of the Examiner's rejection are requested.

Response to Rejections Under 35 U.S.C. 102 & 103 rejections

Claims 1-6 were rejected under 35 U.S.C. 102(e) as being anticipated by Hsieh (USP 6,645,824).

Claims 7-10 and 19-22 were rejected under 35 U.S.C. 102(a) as being unpatentable over Hsieh.

Applicants respectfully assert that Hsieh is legally deficient for the purpose of anticipating claim 1 for the reasons that each and every element of the claim in issue is not found in the prior art reference.

The present invention teaches substantially in claims 1 and 7 a NAND type of non-volatile memory wherein each gate structure comprises, from the substrate, at least a bottom dielectric layer, a charge-trapping layer, an upper dielectric layer, a control gate and a cap layer. The present invention further teaches in claim 3 that the charge-trapping layer comprises silicon nitride.

Although Hsieh teaches an ONO film 130, the ONO film 130 of Hsieh serves as an inter-gate dielectric layer between the floating gate 120 and the control gate 140, rather than as a charge-trapping layer as in the present invention. *See* Hsieh, Col. 7, lines 14-23. In essence, Hsieh teaches a gate structure that contains, from bottom to top, an oxide layer (110), a floating gate (120), an oxynitride film also known as ONO (130), a control gate (140) and a silicon nitride layer (150). *See* Hsieh, Col. 7, Lines 3-49; Col. 8, Lines 27-40 and Figs. 5e and 5f. In contrast, the present invention teaches a gate structure that contains, from bottom to top, a bottom dielectric layer, a charge-trapping layer made of silicon nitride, an upper dielectric layer, a control gate, and a cap layer. *See* Specification, Paras. 31-37 and Fig. 2B. Fundamentally, the charge trapping unit of Hsieh is the polysilicon floating gate (120), whereas the present invention teaches the charge-trapping layer is made from silicon nitride, replacing the FGs in prior art and in Hsieh. Accordingly, Hsieh at least fails to anticipate the non-volatile memory structure of the instant case in this regard.

In addition, Hsieh teaches that the fourth polysilicon layer (220), patterned to define select gates, serves as the word line that is oriented perpendicular to the first and second bit lines.

See Hsieh, Col. 8, Lines 33-35. In contrast, the present invention teaches that the CG line of a NAND type memory should serve as the word line and also teaches the control gate line to be oriented in parallel to the SG lines (bit lines). *See* Specification, Paras. 33-40 and Fig. 3. Therefore, Hsieh does not anticipate claim 1, and the rejection should be withdrawn.

With regard to the 103 rejections of claim 7 by Hsieh, Applicants respectfully submit that these claims defined over the prior art references for at least the reasons discussed above.

If independent claims 1 and 7 are allowable over the prior art of record, then its dependent claims 2-6 and 19 are allowable as a matter of law, because these dependent claims contain all elements of their respective independent claims 1 and 7. Therefore, reconsideration and allowance of the pending claims are requested.

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CONCLUSION

For at least the foregoing reasons, it is believed that the presently pending claims 1-10, 19-22 are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

Respectfully submitted,

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